Physical Observation of a Thermo-Morphic Transition in a Silicon Nanowire

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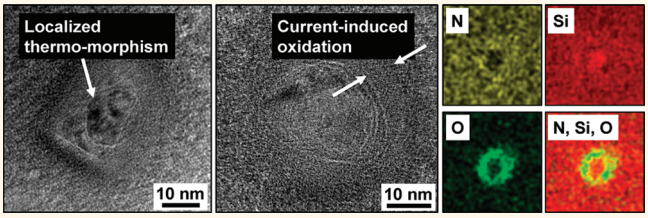
ABSTRACT



A thermo-morphic transition of a silicon nanowire (Si-NW) is investigated in vacuum and air ambients, and notable differences are found under each ambient. In the vacuum ambient, permanent electrical breakdown occurs as a result of the Joule self-heating arising from the applied voltage across both ends of the Si-NW. The resulting current abruptly declines from a maximum value at the breakdown voltage (V_{BD}) to zero. In addition, the thermal conductivity of the Si-NW is extracted from the V_{BD} values under the vacuum ambient and shows good agreement with previously reported results. While the breakdown of the Si-NW does not exhibit negative differential resistance under the vacuum ambient, it interestingly shows negative differential resistance with multiple resistances in the current–voltage characteristics under the air ambient, similar to the behavior of carbon nanotubes. This behavior is triggered by current-induced oxidation, which leads to the thermo-morphic transition observed by TEM analyses. Additionally, the current-induced oxidation is favorably applied to reduce the size of a Si-NW at a localized and designated point.

KEYWORDS: thermo-morphic transition · thermo-morphism · silicon nanowire · electrical breakdown · air ambient · vacuum ambient · Joule heating · self-heating · current-induced oxidation · oxidation · thermal conductivity · multiple resistance

Nanomaterials such as carbon nanotubes (CNTs), nanowires (NWs), nanocrystals, and supramolecular structures have been proposed as the basic building blocks for a new generation of electronic and mechanical systems, including memory and logic components,[1−3] light-emitting devices and photodetectors,[4−6] electromechanical actuators,[7] biosensors,[8] and drug delivery systems.[9] With their small size and high surface-to-volume ratio, nanostructure devices can be faster, cheaper, more efficient, and more sensitive than conventional and bulky devices. Among nanomaterials reported to date, one-dimensional CNTs and NWs have sparked widespread scientific and engineering interest owing to their outstanding electrical properties. On the basis of these properties, their application in integrated circuits (as transistors or interconnects) has been proposed.[10−13] However, a severe power problem can be anticipated with the use of one-dimensional materials, *i.e.*, CNTs or NWs, because high-field transport is significantly affected by the surrounding environment due to reduced dimensionality for thermal conduction and phonon relaxation. Moreover, the extremely scaled size of one-dimensional materials imposes a constraint on their applications owing to vulnerability to electrostatic discharge stresses.[14,15] Accordingly, understanding of their thermal properties is crucial to understanding their overall behavior.

A one-dimensional conductor with a length (L) of tens of micrometers (*i.e.*, when L is much larger than the phonon mean free path) can be regarded as a diffusive conductor because local thermal equilibrium can be achieved in the conductor due to energy relaxation via a scattering process of electrons with phonons.[16,17] Therefore, significantly harsh thermal stress stemming from Joule heating can be generated along the direction of the current flow. Regarding suspended diffusive CNTs, it has been well documented that thermo-morphism (*i.e.*, thermally induced transition of the morphology) near the center region ($\sim L/2$) occurs with current-induced oxidation and localized melting being observed during electrical breakdown.[17−23] Furthermore, for metallic or semiconductor NWs, since their phonon mean free path is typically not longer than tens of nanometers, NWs can also be safely regarded as a diffusive conductor. Recent experimental and theoretical studies on silicon nanowires (Si-NWs), in particular, indicate that as the width of Si-NWs decreases below approximately

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Received for review November 28, 2011 and accepted February 10, 2012.

Published online February 10, 2012
10.1021/nn2046295

150 nm, the thermal conductivity is reduced due to phonon surface scattering.[24−26] Thus, the thermomorphism from significant Joule heating raises further concerns and is expected to be of practical importance for applications of Si-NWs in electronics and integrated circuits. Nevertheless, little is known about thermomorphism from the Joule heating in Si-NWs, especially regarding the electrical breakdown and the current-induced oxidation behaviors.

Here, we empirically investigate thermal properties, thermo-morphic transitions, and localized current-induced oxidation of suspended Si-NWs under both vacuum and air ambients. From the measured breakdown voltage (V_{BD}) values of the Si-NWs under the vacuum ambient, the thermal conductivity of the Si-NWs is extracted and compared with previously reported values for the first time. The breakdown behaviors of the Si-NWs are significantly different for each ambient until reaching a point of electrical failure. Most importantly, it is found that the current-induced oxidation under an air ambient is observed at a localized area ($\sim L/2$), which corresponds to a hot spot caused by Joule self-heating. As a result, current−voltage ($I-V$) characteristics in the air ambient show a domain of negative differential resistance. Moreover, the electrical breakdown occurs with multiple conductance slopes, similar to the behavior of CNTs.

RESULTS AND DISCUSSION

A well-developed top-down approach based on photolithography and etching processes with subsequent size reduction by partial photoresist ashing was used to fabricate Si-NWs on an 8 in. wafer. One of the important advantages of the top-down approach is the ability to precisely and uniformly control size, location, and shape. Additionally, it ensures pattern fidelity even with high throughput. Accordingly, it is possible to systematically investigate the behaviors of the Si-NWs under various conditions. The fabrication process can be briefly summarized as follows: a silicon-on-insulator (SOI) wafer with a silicon film thickness of 40 nm on a buried oxide (BOX) layer of 1 μm was used as a starting material. This was heavily doped by phosphorus with a doping concentration of approximately 3×10^{19} /cm^3, and the Si-NWs were delineated by the aforementioned top-down approach. The patterned Si-NWs have widths ranging from 25 to 145 nm. Overetching of the BOX by use of diluted hydrofluoric acid carved the BOX until the Si-NWs were separated from it. A scanning electron microscopy (SEM) image of a typical suspended Si-NW is shown in the inset of Figure 1A. Measured resistances of the Si-NWs with various widths are also plotted in Figure 1A. The measurement was performed at a low-bias region (*i.e.*, ranging from −0.5 to 0.5 V), thus mitigating effects of the current saturation arising from Joule self-heating on the resistance value. In this regime, the Si-NWs typically exhibit a linear $I-V$ relationship (Ohmic behavior). The thermal isolation of the suspended Si-NWs ensures that the self-heating stemming from Joule heating (referred to hereafter as simply Joule self-heating) is preferentially intensified inside the Si-NWs.

Electrical breakdown is first investigated under a vacuum ambient (approximately 10^{-2} Torr) at room temperature. Figure 1B shows the distribution of the V_{BD} values of the Si-NWs with various widths and a fixed nanowire length (L = 1.3 μm). $I-V$ characteristics were measured with the aid of a parameter analyzer (HP 4155). Increment of voltage leads to increasing input power, which causes the Si-NWs to heat up rapidly because of the concentrated Joule self-heating, hence giving rise to physical and electrical breakdown. In the vacuum ambient, a linear relationship is observed at low bias and a nonlinear trend is seen at high bias (>1.0 V). Note that, regardless of the integration time (here, the integration time is split into 80 μs and 332 ms[27]), electrical breakdown occurred with a current drop characterized by a single slope, *i.e.*, a single valued conductance as shown in the inset of Figure 1B. These behaviors are typical of the breakdown in semiconductor NWs. Moreover, it is found that there is no hysteresis in the $I-V$ behaviors, which are highly reproducible for each iterative voltage sweep from low to high and high to low, excluding when the Si-NWs reach permanent breakdown near 1.5 V. It is noteworthy that nonlinear $I-V$ characteristics are not observed when the Si-NW is not suspended from the substrate, because the heat generated from the strong electron scattering involved with optical phonons can be easily dissipated through the substrate (Supporting Information Figure S1).[16,23,28] Accordingly, the nonlinearity at high bias can be primarily attributed to the self-heating effect. The self-heating effect generally becomes more significant as the width of the Si-NW narrows due to the aforementioned reduced thermal conductivity (κ).[24−26] As a result, the V_{BD} is rapidly reduced with a decrease of the width, as shown in Figure 1B, because the generated heat cannot escape readily and outwardly from the narrow Si-NW in the case of a suspended Si-NW under a vacuum ambient.

A generalized heat conduction equation along the direction of the current flow in a one-dimensional (1-D) suspended NW, which includes the heat generation from Joule self-heating, is given by[16,17]

$$A\nabla[\kappa\nabla T(x)] + p = 0 \qquad (1)$$

where A is the cross-sectional area of the conductor, $T(x)$ is the temperature profile along the current-flow direction, and p is the Joule heating rate per unit length. Generally, p is expressed as $p = (IV - I^2R_c)/L$, where R_c is the total contact resistance; however, it is typically much smaller than the resistance of a 1-D nanowire. Therefore, R_c can be neglected, *i.e.*, $p \approx IV/L$.

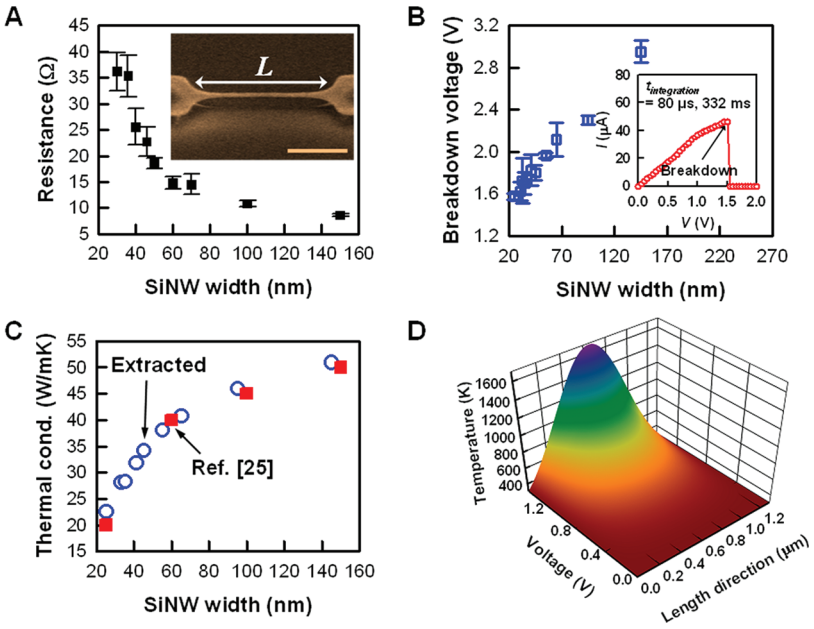

Figure 1. (A) Resistance of the suspended Si-NWs with widths ranging from 25 to 145 nm and a length of 1.3 μm. (Inset) SEM image of a suspended Si-NW with a width of 25 nm and a length of 1.3 μm. Scale bar is 500 nm. (B) Electrical V_{BD} values of different suspended Si-NWs in a vacuum ambient. (Inset) Current−voltage ($I-V$) characteristic of a suspended Si-NW with a width of 25 nm and a length of 1.3 μm at room temperature measured in a vacuum ambient. Regardless of integration time, the $I-V$ characteristics result in the same behavior. (C) Extracted thermal conductivities of Si-NWs having different widths. The thermal conductivity values from experiments are taken from ref 25. (D) Predicted distribution of the temperature in the suspended Si-NW according to the bias conditions.

Here, the temperature is determined by the Joule power dissipated along the Si-NW and by its thermal conductivity, as delineated in eq 1. This provides physical insight into the electro-thermal behavior of the Si-NW at high bias and explains how the thermal conductivity is directly linked to the measured electrical characteristics at high bias. It was reported that the thermal conductivity based on experiments could be modeled as follows:[16,17,29] $\kappa = 1/(\alpha T + \beta T^2)$, where the linear term (αT) represents the Umklapp scattering and the quadratic term (βT^2) expresses second-order three-phonon processes. Here α and β are constants. From this empirical equation, an analytical temperature profile satisfying eq 1 is attained as a closed form.[29] The breakdown temperature (T_{max}) is thus obtained at the middle of the 1-D nanowire by considering the Umklapp scattering (*i.e.*, $\kappa = 1/\alpha T$):

$$T_{max} = T_0 \exp\left(\frac{\alpha I_c V L}{8A}\right) \quad (2)$$

where T_0 is the temperature at the contact electrodes and I_c is the critical breakdown current. Using a melting point of 1687 K for bulk silicon, the thermal conductivity of the Si-NW and its temperature profile are simply extracted from the electrical measurement for the first time. Figure 1C shows the estimated thermal conductivity for various widths of the Si-NW at room temperature. The results are also compared with those from the experiments as well as numerical simulations reported by other groups,[24−26] and good agreement is observed. In addition, the predicted temperature profile of a Si-NW with a width of 25 nm at different bias conditions is shown in Figure 1D, revealing that the temperature in the Si-NW ranges from approximately 900 to 1000 K at around 1.1 V, where the nonlinearity first appears. When the bias is further increased, the Si-NW is electrically broken at 1.5 V, at which point the temperature corresponds to 1687 K.

Similar experiments were performed under an air ambient. Several notable differences were observed under the air ambient compared to under the vacuum ambient (Figure 2A). A negative differential resistance (NDR) region was clearly observed after the region exhibiting a nonlinearity around 1.0 V. Furthermore, the NDR characteristic becomes more prominent as the integration time is increased. Moreover, a further increase of the voltage leads to electrical breakdown with multiple resistances in the $I-V$ characteristics for prolonged integration time, which is somewhat similar to the pattern of breakdown in multiwalled CNTs.[18−20] On the contrary, such behaviors were not observed with shortened integration time (to be discussed in detail later). From the SEM images taken from two Si-NW samples (a pristine Si-NW and a Si-NW at 1.6 V with long integration time), we clearly observed a physical transition by thermo-morphism in a suspended Si-NW for the first time. It is inferred that this structural modification in the air ambient is caused by the localized current-induced oxidation, which is triggered by the significant Joule self-heating. Moreover, a

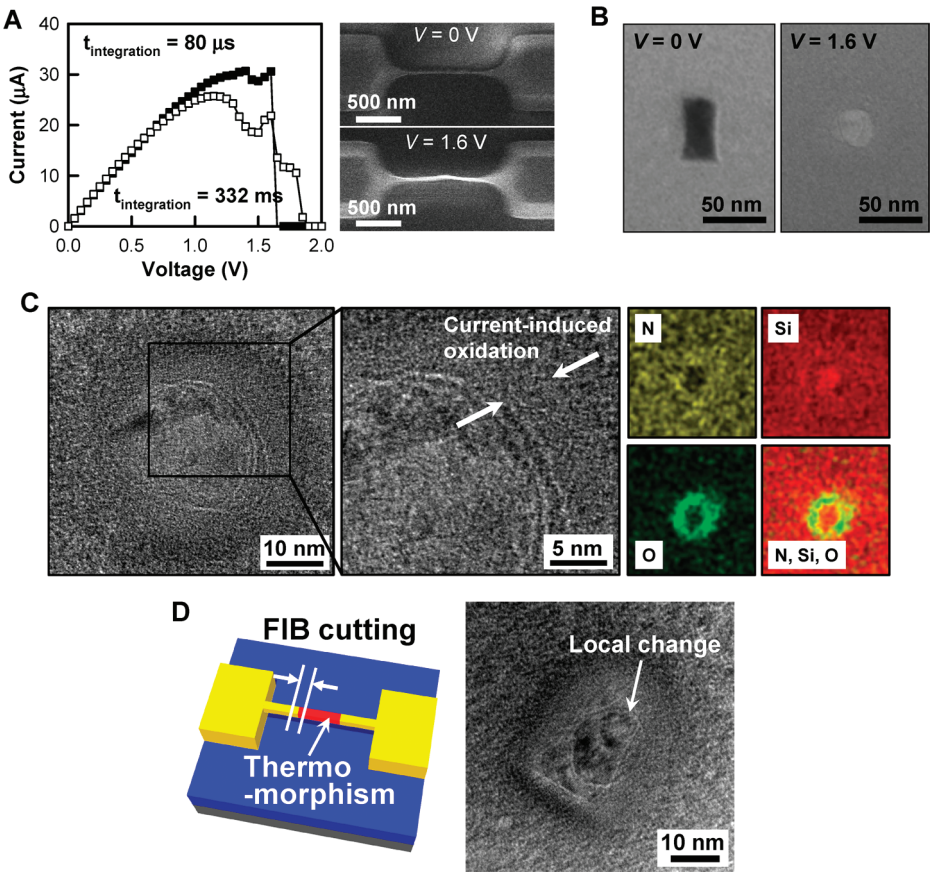

Figure 2. (A) Current−voltage characteristics of suspended Si-NWs with a width of 25 nm and a length of 1.3 μm in an air ambient. The filled and empty symbols represent the measured data with integration time of 80 μs and 332 ms, respectively. The SEM images correspond to the Si-NWs at different bias conditions for long integration time. (B) Cross-sectional TEM images of the Si-NW around the center region for different bias conditions. (C) Magnified bright-field TEM image of the Si-NW around the center region after electrical breakdown. Moreover, EDS mapping data ensure the outer shell-oxide (O: green) and the inner core-Si (Si: red). N (yellow) comes from the passivation layer of SiN_x for the TEM sample preparation. (D) Cross-sectional TEM image showing an overlapped profile of the circular and the rectangular structures. The circular shape corresponds to the central region of the Si-NW, and the rectangular shape corresponds to the Si-NW near the electrode.

notable structural change from a rectangular to circular cross-sectional profile by the thermo-morphism is found near the central part ($\sim L/2$) of the Si-NW in the case of long integration time (Figure 2B), possibly due to a sequential process of current-induced oxidation, melting, and resolidification. As discussed previously, the temperature around the center of the Si-NW is high enough (*i.e.*, 900−1000 K at around 1.1 V) to enable local oxidation by an oxidant (oxygen) from air. Therefore, we interpret the NDR behavior shown in the $I-V$ characteristics to be a signature of the reduced width of the Si-NW by the consumption of the silicon during the current-induced oxidation. As a result, a unique structure comprised of a shell-oxide and a core-silicon is created after applying electrical bias under an air ambient.

As it is very important to verify the existence of the local oxide, cross-sectional energy dispersive X-ray spectroscopy (EDS) element mapping was carried out in an effort to trace the thermo-morphic transition of the Si-NW during a TEM analysis. The results confirm that the local oxide encapsulates a core of the Si-NW, as shown in Figure 2C. Moreover, a further TEM analysis was carried out to present clear evidence of the localized thermo-morphic transition in the Si-NW through delicate preparation of the Si-NW sample, which was cut between the rectangular and circular regions by a focused ion beam (FIB). Both the rectangular (undamaged by Joule self-heating) and the circular (damaged by Joule self-heating) images are distinctly overlapped because of transmitted electrons through the extremely thin TEM sample, as shown in Figure 2D. It is therefore confirmed that the thermo-morphic transition is seen only near the Si-NW center, enabling us to visibly observe that the Si-NW is a diffusive conductor.

A suspended single-wall CNT also exhibited clear NDR behavior,[16,23,28] but its characteristics are comprehensively different from those of the Si-NW. In the single-wall CNT, there was no hysteresis in the $I-V$ characteristics according to iterative biasing after the NDR action was triggered. However, distinctive hysteresis by each iterative biasing was observed in the Si-NW after the NDR operation was enabled, as shown in

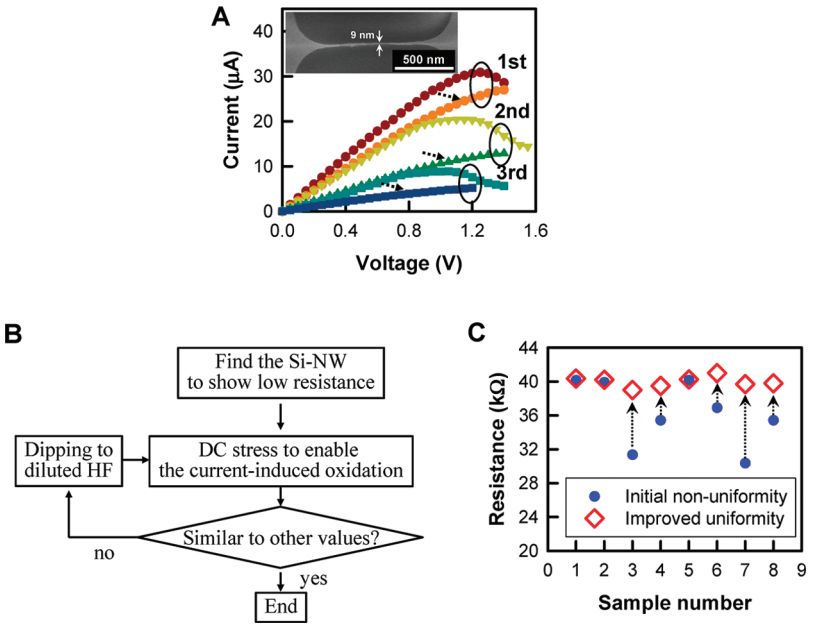

Figure 3. (A) *I*–*V* characteristics of the suspended Si-NW during iterative current-induced oxidation. The dotted arrows indicate the successive measured *I*–*V* data immediately after each current-induced oxidation. Note that the NDR region disappears. (Inset) SEM image of the Si-NW (9 nm width) after the third current-induced oxidation and etching processes. (B) Block diagram of the width engineering method to establish uniformly distributed resistance of the Si-NWs by current-induced oxidation, which enables width engineering. (C) Resistance of the Si-NWs before and after width engineering.

Figure 3A. Voltage sweep was intentionally halted in the NDR region, and thereafter the *I*–*V* characteristics were measured again. It should be noted that the NDR behavior disappears after the intentional cessation of the applied voltage in the NDR region after each sweep (indicated by the dotted arrow in Figure 3A). This can be ascribed to saturation of the oxidation rate by the stress-limited oxidation[30] and lowered oxygen diffusivity inside the shell-oxide. After the first voltage sweep, the current-induced oxide is etched away by diluted hydrofluoric acid. In the consecutive second voltage sweep, the current-induced oxidation occurred again. Note that the bias at which the NDR region appears is lowered at the consecutive voltage sweep, resulting from the reduced width of the Si-NW. With further iterative oxidation by Joule self-heating, the size of the 25 nm Si-NW is reduced to a diameter of 9 nm (inset of Figure 3A). Similar characteristics of current-induced oxidation were also observed in the multiwalled CNTs, wherein each shell was removed by the current-induced oxidation. To the best of our knowledge, this is the first demonstration of the localized current-induced oxidation in a Si-NW. Our observations support that current-induced oxidation governed by Joule self-heating can be a powerful tool to reduce the size of NWs and to grow an oxide layer at an extremely localized and designated area. Additionally, the large fluctuation of resistance in the Si-NWs is reduced by application of selective bias to individually addressable Si-NWs (Figure 3B). Uniformly distributed resistance is consequently achieved by employment of selective current-induced oxidation controlled electrically rather than chemically.

To systematically induce Joule self-heating to the Si-NW by dc stress, current is measured as a function of time at a fixed bias (Figure 4A). Voltage sweep is started from 0 V at every 0.05 V and intentionally halted for 5 s from 0 to 1.0 V and 10 s from 1.05 to 1.9 V in order to read the time-dependent current at fixed bias. In a range of 0 to 1.1 V (*i.e.*, the cumulated time is 120 s), the time dependence of the current at each step is negligible, indicating that the conductance of the Si-NW is sustained reliably. Above 1.1 V, however, the current decay rate (d*I*/d*t*) starts to increase, similar to observations reported from CNTs.[20] The onset of the current decay at 1.1 V can be taken as an indication of the start of oxidation in the Si-NW. With further increase of the dc bias, d*I*/d*t* is decreased again, indicating that the current-induced oxidation is saturated (inset of Figure 4A). Beyond the critical point (1.3 V, *i.e.*, the cumulative time is 151 s), therefore, further increment of dc bias results in a decrease of the current decay rate and a gradual increase of the current.

Another striking feature in Figure 4A is that the electrical breakdown shows multiple resistance steps until the Si-NW reaches permanent electrical failure, which appears from 1.5 V. This behavior is analogous to that of multiwalled CNTs under an air ambient in that the shell-by-shell electrical breakdown is completed via multiple resistance steps,[18–20] although each resistance step in the case of the Si-NW is not as distinctive as that at the multiwalled CNTs. Furthermore, it is found that the Si-NW is electrically discontinuous with a single declining slope of the current under the vacuum ambient (Supporting Information

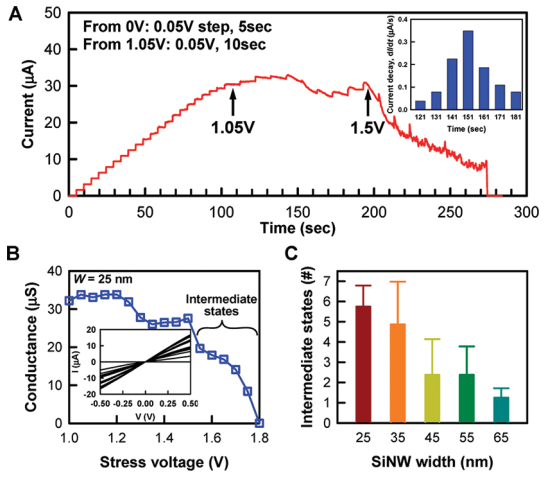

Figure 4. (A) Current as a function of time at certain temporarily fixed bias voltages. (Inset) Plot of the current decay rate (d*I*/d*t*) *versus* time at fixed voltages (*V*). The bell-shaped curve indicates that the current-induced oxidation is almost saturated. (B) Conductance *versus* dc stress voltage characteristics of the suspended Si-NW. The conductance is extracted from the current−voltage characteristics at low bias shown in the inset figure after each dc stress. (C) Statistical distribution of the number of intermediate states in Si-NWs with different widths. The number of intermediate states is extracted from the plot of the conductance *versus* the dc stress voltage characteristics.

Figure S2), whereas it is electrically broken with multiple declining slopes of the current under the air ambient. This reveals that the current-induced oxidation plays a dominant role in leading the electrical breakdown with multiple resistances. Moreover, the observation that electrical breakdown with a single slope was not found at short integration time (Figure 2A) even under the air ambient can be understood in that the dc biased time was not sufficient to trigger current-induced oxidation by Joule self-heating. Although a comprehensive understanding of this new observation requires further investigation, it is interesting to note that the Si-NWs behave like CNTs during the electrical breakdown. It is speculated that this behavior originates from the unique structure of the shell-oxide and core-silicon near half of the length of the Si-NW. Since silicon oxide (SiO_x) generally begins to melt at approximately 2000 K, which is higher than the melting point of the bulk silicon, the shell-oxide can prevent the Si-NW from being melted down, hence preventing its fracture. Furthermore, reflow and solidification of the melted core-silicon inside the shell-oxide might give rise to variation of the crystallinity of the Si-NW from single-crystalline to polycrystalline and/or an amorphous structure, possibly resulting in a decrease of the conductance during electrical breakdown. This can be supported in part by the absence of a well-ordered silicon lattice in the relevant TEM image, shown in Figure 2C.

Our observations indicate that the present Si-NW showing multiple resistance states can be used for memory applications. After high dc bias is applied to the Si-NW for program operation, the resistance (or conductance) is accordingly changed as shown in Figure 4B. Thereafter, a linear relationship is sustained with various resistance states as long as low dc bias (*e.g.*, −0.5 to 0.5 V) is applied for read operation. These different resistance states are distinctive from each other, as shown in the inset of Figure 4B, and therefore can also be applicable to neuro-morphic devices. It should be noted that the controlled conductance after the supply of high dc bias shows remarkably sustainable conductance states even after 10^5 s (Supporting Information Figure S3). This data sustainability can represent a step toward the application of a multibit per cell in nonvolatile memory or a write-once read-many-times (WORM) memory.[31] The number of distinctive data states increases as the width of the Si-NW is reduced, as shown in Figure 4C, because a thicker Si-NW cannot be distinctly oxidized, possibly resulting in a sudden fracture of the Si-NW by Joule self-heating. Therefore, this feature can be exploited to accommodate more data states at further scaled Si-NWs.

CONCLUSIONS

In summary, a thermo-morphic transition induced by Joule self-heating was experimentally observed in a Si-NW for the first time. Thermal properties driven by the Joule heat were investigated under vacuum and air ambients. By analyzing the electrical breakdown in Si-NWs under a vacuum ambient, we extracted the thermal conductivity and the temperature profile of Si-NWs, enabling estimation of the thermal properties of a Si-NW. Importantly, we found that the significant Joule self-heating resulted in localized current-induced oxidation under an air ambient. Evidence showing the outer shell-oxide and inner core-Si created by the localized current-induced oxidation was provided from EDS element mapping data. The current-induced oxidation led to negative differential resistance in the *I*−*V* characteristics. Furthermore, the current-induced oxidation was also utilized to reduce the size of the Si-NW and to grow an oxide at a localized and designated area. Due to the locally grown oxide created from Joule self-heating, the electrical breakdown of a Si-NW in an air ambient showed similar trends to CNTs in terms of breakdown behavior with multiple resistance steps. This unique characteristic can be applied to a multibit per cell of nonvolatile memory or a write-once read-many-times memory.

Conflict of Interest: The authors declare no competing financial interest.

Acknowledgment. This research was supported by the National Research Foundation of Korea funded by the Korean government (grant number 2011-0020487), the Nano-Material Technology Development Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Education, Science and Technology (grant number 2011-0019120), the IT R&D program of MKE/KEIT (10035320,

Development of Novel 3-D Stacked Devices and Core Materials for the Next Generation Flash Memory), and Samsung Electronics Company, Ltd.

Supporting Information Available: Detailed current–voltage characteristics for clamped as well as suspended silicon nanowires, current *versus* dc stress characteristics under a vacuum ambient, and sustainability of multiple conductance states. This material is available free of charge *via* the Internet at http://pubs.acs.org.

REFERENCES AND NOTES

1. Rueckes, T.; Kim, K.; Joselevich, E.; Tseng, G. Y.; Cheung, C. L.; Lieber, C. M. Carbon Nanotube-Based Nonvolatile Random Access Memory for Molecular Computing. *Science* **2000**, *289*, 94–97.
2. Bachtold, A.; Hadley, P.; Nakanishi, T.; Dekker, C. Logic Circuits with Carbon Nanotube Transistors. *Science* **2001**, *294*, 1317–1320.
3. Tans, S. J.; Verchueren, A. R. M.; Dekker, C. Room-Temperature Transistor Based on a Single Carbon Nanotube. *Nature* **1998**, *393*, 49–52.
4. Huang, M. H.; Mao, S.; Feick, H.; Yan, H. Q.; Wu, Y. Y.; Kind, H.; Webber, E.; Russo, R.; Yang, P. D. Room-Temperature Ultraviolet Nanowire Nanolasers. *Science* **2001**, *292*, 1897–1899.
5. Misewich, J. A.; Martel, R.; Avouris, P.; Tsang, J. C.; Heinze, S.; Tersoff, J. Electrically Induced Optical Emission from a Carbon Nanotube FET. *Science* **2003**, *300*, 783–786.
6. Wang, J. F.; Gudiksen, M. S.; Duan, X. F.; Cui, Y.; Lieber, C. M. Highly Polarized Photoluminescence and Photodetection from Single Indium Phosphide Nanowires. *Science* **2001**, *293*, 1455–1457.
7. Fennimore, A. M.; Yuzvinsky, T. D.; Han, W. Q.; Fuhrer, M. S.; Cumings, J.; Zettl, A. Rotational Actuators based on Carbon Nanotubes. *Nature* **2003**, *424*, 408–410.
8. Cui, Y.; Wei, Q.; Park, H.; Lieber, C. M. Nanowire Nanosensors for Highly Sensitive and Selective Detection of Biological and Chemical Species. *Science* **2001**, *293*, 1289–1292.
9. Sershen, S. R.; Westcott, S. L.; Halas, N. J.; West, J. L. Temperature-Sensitive Polymer–Nanoshell Composites for Photothermally Modulated Drug Delivery. *J. Biomed. Mater. Res.* **2000**, *51*, 293–298.
10. Cui, Y.; Zhong, Z.; Wang, D.; Wang, W. U.; Lieber, C. M. High Performance Silicon Nanowire Field Effect Transistors. *Nano Lett.* **2003**, *3*, 149–152.
11. Singh, N.; Agarwal, A.; Bera, L. K.; Liow, T. Y.; Yang, R.; Rustagi, S. C.; Tung, C. H.; Kumar, R.; Lo, G. Q.; Balasubramanian, N.; Kwong, D.-L. High-Performance Fully Depleted Silicon Nanowire (Diameter $\leq$ 5 nm) Gate-All-Around CMOS Devices. *IEEE Electron. Device Lett.* **2006**, *27*, 383–386.
12. Javey, A.; Qi, P.; Wang, Q.; Dai, H. Ten- to 50-nm-Long Quasi-Ballistic Carbon Nanotube Devices Obtained without Complex Lithography. *Proc. Natl. Acad. Sci.* **2004**, *101*, 13408–13410.
13. Kreupl, F.; Graham, A. P.; Duesberg, G. S.; Steinhögl, W.; Liebau, M.; Unger, E.; Hönlein, W. Carbon Nanotubes in Interconnect Applications. *Microelectron. Eng.* **2002**, *64*, 399–408.
14. Pop, E.; Mann, D.; Wang, Q.; Goodson, K.; Dai, H. J. Thermal Conductance of an Individual Single-Wall Carbon Nanotube above Room Temperature. *Nano Lett.* **2006**, *6*, 96–100.
15. Voldman, S. Nano Electroststic Discharge. *IEEE Nanotechnol. Mag.* **2009**, *3*, 12–15.
16. Liu, W.; Liou, J. J.; Jiang, Y.; Singh, N.; Lo, G. Q.; Chung, J.; Jeong, Y. H. Failure Analysis of Si Nanowire Field-Effect Transistor Subject to Electrostatic Discharge Stresses. *IEEE Electron. Device Lett.* **2010**, *31*, 915–917.
17. Begtrup, G. E.; Ray, K. G.; Kessler, B. M.; Yuzvinsky, T. D.; Garcia, H.; Zettl, A. Probing Nanoscale Solids at Thermal Extremes. *Phys. Rev. Lett.* **2007**, *99*, 155901.
18. Collins, P. G.; Hersam, M.; Arnold, M.; Martel, R.; Avouris, P. Current Saturation and Electrical Breakdown in Multiwalled Carbon Nanotubes. *Phys. Rev. Lett.* **2001**, *86*, 3128–3131.
19. Collins, P. G.; Arnold, M. S.; Avouris, P. Engineering Carbon Nanotubes and Nanotube Circuits Using Electrical Breakdown. *Science* **2001**, *292*, 706–709.
20. Mølhave, K.; Gudnason, S. B.; Pederson, A. T.; Claussen, C. H.; Horsewell, A.; Bøggild, P. Transmission Electron Microscopy Study of Individual Carbon Nanotube Breakdown Caused by Joule Heating in Air. *Nano Lett.* **2006**, *6*, 1663–1668.
21. Huang, J. Y.; Chen, S.; Jo, S. H.; Wang, Z.; Han, D. X.; Chen, G.; Dresselhaus, M. S.; Ren, Z. F. Atomic-Scale Imaging of Wall-by-Wall Breakdown and Concurrent Transport Measurements in Multiwall Carbon Nanotubes. *Phys. Rev. Lett.* **2005**, *94*, 236802.
22. Yuzvinsky, T. D.; Mickelson, W.; Aloni, S.; Konsek, S. L.; Fennimore, A. M.; Begtrup, G. E.; Kis, A.; Regan, B. C.; Zettl, A. Imaging the Life Story of Nanotube Devices. *Appl. Phys. Lett.* **2005**, *87*, 083103.
23. Pop, E.; Mann, D.; Cao, J.; Wang, Q.; Goodson, K.; Dai, H. Negative Differential Conductance and Hot Phonons in Suspended Nanotube Molecular Wires. *Phys. Rev. Lett.* **2005**, *95*, 155505.
24. Li, D.; Wu, Y.; Kim, P.; Shi, L.; Yang, P.; Majumdar, A. Thermal Conductivity of Individual Silicon Nanowires. *Appl. Phys. Lett.* **2003**, *83*, 2934–2936.
25. Chen, Y. F.; Li, D. Y.; Lukes, J. R.; Majumdar, A. Monte Carlo Simulation of Silicon Nanowire Thermal Conductivity. *J. Heat Transfer* **2005**, *127*, 1129–1137.
26. Hochbaum, A. I.; Chen, R.; Delgado, R. D.; Liang, W.; Garnett, E. C.; Najarian, M.; Majumdar, A.; Yang, P. Enhanced Thermoelectric Performance of Rough Silicon Nanowires. *Nature* **2008**, *451*, 163–168.
27. Integration time in the parameter analyzer is defined as the time to take some measurement samples. Thereafter, the parameter analyzer averages the measurement samples and obtains the final measurement data for reduction of equipment errors. Therefore, setting a longer integration time increases the time for inducing the voltage as a result of the increase of the number of samples.
28. Pop, E. Energy Dissipation and Transport in Nanoscale Devices. *Nano Res.* **2010**, *3*, 147–169.
29. Huang, X. Y.; Zhang, Z. Y.; Liu, Y.; Peng, L.-M. Analytical Analysis of Heat Conduction in a Suspended One-Dimensional Object. *Appl. Phys. Lett.* **2009**, *95*, 143109.
30. Kedzierski, J.; Bokor, J.; Kisielowski, C. Fabrication of Planar Silicon Nanowires on Silicon-on-Insulator Using Stress Limited Oxidation. *J. Vac. Sci. Technol. B* **1997**, *15*), 2825–2828.
31. Moller, S.; Perlov, C.; Jackson, W.; Taussig, C.; Forrest, S. R. A Polymer/Semiconductor Write-Once Read-Many-Times Memory. *Nature* **2003**, *426*, 166–169.